Pipeline Architecture

Pipeline
Data Hazards
Branch Hazards
INSTRUCTION FETCH
INSTR DECODE
REG FETCH
EXECUTE/
ADDRESS CALC
MEMORY
ACCESS
WRITE
BACK

PC
Instruction
Memory

4
ADD

Instruction
Memory

write
Registers

Sign Ext

ALU

write
read
Data
Memory

ALU CTRL

CONTROL

MUX

MUX

MUX

MUX

MUX

MUX

MUX

MUX
INSTRUCTION FETCH

INSTR DECODE
REG FETCH

EXECUTE/
ADDRESS CALC

MEMORY
ACCESS

WRITE BACK

PC

Instruction Memory

Instruction Memory

Registers

Registers

ALU

ALU

Data Memory

Data Memory

write
read

write

write

read

INSTRUCTION FETCH

INSTR DECODE
REG FETCH

EXECUTE/
ADDRESS CALC

MEMORY
ACCESS

WRITE BACK

Sign Ext

Sign Ext

ALU CTRL

ALU CTRL

MUX

MUX

MUX

MUX

MUX

MUX

MUX
PC instruction memory registers. Sign Ext MUX. Data memory MUX. Instruction Memory. Registers. ALU CTRL. ADD write read. ALU. Sign Ext. IF ID/RF EXE MEM WB.
Data Hazards

- Software: nop
- Hardware: stall
PC Instruction Memory

Registers

Sign Ext

ALU

CTRL

write read

Data Memory

write

4

ADD

MUX

MUX

MUX

MUX

MUX

MUX

MUX

MUX

MUX
Branch Hazard
Branch Hazard

Accelerate Branch Target Computation

Accelerate Branch Detection