Memory Devices

Latches and Flip-flops
Clocks

• Regular Pulses of High and Low Voltage
• Triggers memory elements
  – on level (high or low)
  – on edge (rising or falling)
S-R Latch (Set - Reset)

- **High**
- **Low**

Set

R → Q
S → ~Q
D Latch (Data Latch)
Flip-Flop (Falling Edge Trigger)

How many transistors?
Register

- Storage for a string of bits
  - number of bits in general register is word size
- Implemented as one flip-flop for each bit
- Output
  - output lines are always available to be read
  - general registers commonly selected by multiplexors
- Input
  - new values may be saved only when signaled by clock
  - select or enable line may control clock line
  - general registers commonly selected for write by decoder
Register  8 bit example
Register file  4 registers

Clock

From Decoder

Data In

To MUX
ARMv8 Register file

- Reg 1 Read
- Reg 2 Read
- Reg Write
- Write Data
- Read Data 1
- Read Data 2
- Write Enable
- Clock